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Review on Data Encoding Scheme for Power Reduction in NOC

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Abstract- As technology shrinks,the power consumed by the links of a network on chip. In this paper we present the data encoding schemes aimed at to reduce the power dissipated by the links of an NoC. The praposed shceme gives the advanced architecture and general and transparent with respect to the underlying NoC fabric.experiments carried out on both synthetic and real traffic scenarios show the3 effectiveness of the praposed schemes which allow to save up to more than 51% of the power dissipation and 14% energy consumption without any significant performance degradation and with less than 15% area overhead in the NI.

Index Terms- Network-on-chip (NoC), Coupling switching activity, data encoding, low power, Interconnection on chip, Power analysis.

1. INTRODUCTION

As the number of IP cores integrated into system SOC increases, role of interconnection system become more and more important because these are the limiting factor for the performance and power in current and next generation SOC. As number of cores increases, total length of interconnection wires increases resulting in long transmission delay, larger area and higher power consumption. Another problem is length of wires decreases with technology in turn it will increase coupling capacitance and height of wire material increases resulting in fringe capacitance. In multi core era, as number of cores increases significantly on SOC, communication system also need to change to support multi core communication demands NOC is solution to scalability issue of future many core system[7].

As the number and heterogeneity of cores into a SOC increases, the use of an adequate communication infrastructure based on the NOC paradigm is generally seen as the most effective solution to deal with the complexity of designing next generation of many-cores architectures. The importance of interconnects complex many-cores chips has outrun the importance of Transistors as a dominant factor of performance, power, cost and reliability Sophisticate on-chip communication protocols, involving advanced adaptive routing algorithms, selection policies, data protection schemes and mechanisms aimed at guarantee the quality-of-service are pushing the interconnect system to become one of the main elements which characterizes the system in terms of both power dissipation and energy consumption.

NOC makes chip architecture highly scalable, and well-controlled electric parameters of the modular block improve the reliability and operation frequency of the on-chip interconnection network. The interconnect systems have become the main element which characterizes the system in terms of both power dissipation and energy consumption.

Dynamic power dissipation in interconnects is a major contributor to power consumption in NOC links. This is mainly due to two factors, self switching activity of the particular link and coupling switching activity among adjacent links dissipate power due to the switching activity both self and coupling induced by subsequent data patterns traversing the link The interconnection network dissipates a significant fraction of the total system power budget. The requirements for encoding are very tight[8]. Since an encoder and decoder has to be implemented on each of the NI of every router, the area overhead has to be tiny and, obviously, these blocks should be power efficient and must not harm performance. In recent years, as SOC design research is actively conducted, a large number of IP are included in one system through network on chip. The real effort and time in using NOC is spent in developing network interfaces (NI) for connecting cores to the NOC. The area and power of NIs should be small and its latency must be kept as low as possible. To reduce power dissipation NIs, we suppose to employ many techniques able to hibernate switching while no communication is available. In this paper, we try to reduce the power dissipation of NOC by reducing the network interface power. We present a hardware design of a low power Network interface design. The low

power is obtained by the implementation of a mechanism based on stoppable clock technique for power saving. There are several works in literature which deal with power dissipation and energy consumption issues in NOC architectures. They differ by either the level of abstraction in which they operate or by the specific NOC element they focus on. In this paper we are focusing on the power dissipated by network links.

2. LITERATURE REVIEW

Deepa N.Sarma et.al. in paper[1] entitled "A Novel Encoding Scheme For Low Power in NOC links" proposed on the power reduction in between the links. Dynamic power dissipation in interconnects is a major contributor to power consumption in Network on Chips (NOCs). This is mainly due to two factors, self switching activity of the particular link and coupling switching activity among adjacent links. Two novel techniques are proposed to reduce power consumption due to switching transition and crosstalk. First technique reorders the data in such a way that switching transition is brought down. In the second technique, it is ensured that power consumption due to cross coupling activity is reduced. Encoder and Decoder exhibiting the proposed scheme have been described in RTL level in Verilog HDL, synthesized and mapped into UMC180 nm technology library.

It has been observed that the proposed technique (TSC) offers an average reduction in dynamic power consumption of 17.34%. Proposed scheme was compared with existing techniques and observations concluded that there was not much degradation in area, speed and static power dissipation[1]. Power reduction when subjected to different kinds of data streams was analyzed and results indicate that proposed scheme offers uniform power reduction irrespective of the nature of data stream unlike the existing techniques. In this paper, two encoding techniques are proposed to reduce power consumption due to self switching activity and crosstalk in NOC links. A two stage encoding scheme incorporating the proposed techniques has been devised. The proposed encoding structure has been implemented and its performance is compared with BI, CDBI and SC encoders. Our module has been tested against different types of data streams and it was observed that unlike other schemes uniform power reduction is guaranteed in all cases. An average power reduction of 17.34% has been obtained..

M.Venkata Theertha et.al in paper[2] entitled "SCDBI Encoding Scheme for NOC Links" proposed on the power reduction and impact on area is very less. The data encoding scheme exploits the wormhole switching techniques and works on an end-to-end basis. That is, flits are encoded by the network interface (NI) before they are injected in the network and are decoded by the destination NI. This makes the scheme transparent to the underlying network since the encoder and decoder logic is integrated in the NI and no modification of the routers architecture is required Data encoding schemes are other techniques to reduce switching power in NOC links by reducing self transition and coupling transition in links. This paper proposed data encoding scheme called self and coupling driven bus invert (SCDBI). By using this method we can reduce the switching power by 34.64% without any significant degradation in area and performance. The SCDBI Encoding Scheme gives better power reduction in between the links.

The power dissipated by the links of a NOC contribute significant fraction of the total power budget. This paper proposed the use of data encoding techniques as a viable way to reduce power dissipation in NOC links. The SCDBI scheme is transparent because they operate on an end-to-end basis and no need to modify the router architecture, only the NI is to be augmented with the encoder and decoder. Although, it represents an overhead, does not introduce a significant penalty both in terms of cost (i.e., silicon area) and latency. The simulation results and synthesis results have shown that, by using the SCDBI encoding scheme it is possible to reduce the power contribution of both the self switching activity and the coupling switching activity in inter-routers links. Precisely, as compared to a baseline implementation in which no data encoding techniques are used, a reduction of up to 34.64% of power dissipation has been observed without any significant degradation in terms of both performance and silicon area[2].

Maurizio Palesi et.al in paper[3] entitled "Data Encoding Schemes in Networks on Chip" proposed the use of data encoding techniques as a viable way to reduce both power dissipation and energy consumption of NOC links. The proposed encoding scheme exploits the wormhole switching techniques and works on an end-to-end basis. That is, flits are encoded by the network interface (NI) before they are injected in the network and are decoded by the destination NI. This makes the scheme transparent to the underlying network since the encoder and decoder logic is integrated in the NI and no modification of the routers architecture is required. We assess the proposed encoding scheme on a set of representative data streams (both synthetic and extracted from real applications) showing that it is possible to reduce the power contribution of both the self-switching activity and the coupling switching activity in inter-routers links.

As results, we obtain a reduction in total power dissipation and energy consumption up to 37% and 18%, respectively, without any significant degradation in terms of both performance and

silicon area. The proposed schemes are transparent to the underlying NOC infrastructure as they operate on an end-to-end basis. No modification of the router architecture is needed as well as links width. Only the NI is augmented with the encoding/decoding logic that, although represents an overhead, does not introduce a significant penalty both in terms of cost (i.e., silicon area) and latency.

The proposed encoding schemes have been compared with several encoding schemes proposed in literature on a set of representative data streams both synthetic and extracted from real applications[3]. The experimental analysis shown that by using the proposed encoding schemes it is possible to reduce the power contribution of both the self switching activity and the coupling switching activity in inter-routers links.

Nima Jafarzadeh et.al in paper[4] entitled "Data Encoding Techniques for Reducing Energy Consumption in Network-on-Chip" proposed efficient power reduction than the previous paper. This paper presented a set of data encoding schemes aimed at reducing the power dissipated by the links of NOC. The proposed schemes are general and transparent with respect to the underlying NOC fabric. Experiments carried out on both synthetic and real traffic scenarios show the effectiveness of the proposed schemes, which allow to save up to 51% of power dissipation and 14% of energy consumption without any significant performance degradation and with less than 15% area overhead in the NI.

The proposed encoding schemes are agnostic with respect to the underlying NOC architecture in the sense that their application does not require any modification neither in the routers nor in the links. An extensive evaluation has been carried out to assess the impact of the encoder and decoder logic in the NI. The encoders implementing the proposed schemes have been assessed in terms of power dissipation and silicon area. The impacts on the performance, power, and energy metrics have been studied using a cycle- and bit accurate NOC simulator under both synthetic and real traffic scenarios[4].

Now we will be also focusing on data encoding scheme which will give an effective power reduction in NOC Links. We will use the same encoding but modifying the architecture of the encoder. We are targeting the three factors that are power reduction, energy consumption and less area. By modifying the architecture of the encoder scheme we can achieve the target.

3. EXPERIMENTAL STUDY

We will be using the methodology of transition data and using 65-nm UMC technology. Our aim is to reduce the power, energy and area. For that we are using the new methodology by changing the architecture of the encoder scheme. It is proposed to change the architecture by using the D flip flop or by T flip flop. The D latch or T latch can also be used. As in the previous architecture the different links are connected and we will get the output on the different links in different times. In this case it dissipates much more power in that links. In previous paper we use the X-OR gates and out-put in different links at random time it dissipates the more power. So we are modifying this architecture and try to collect the output on a single link so power will reduce.

We can achieve this by using D flip flop and X-OR gates or replace this by using T flip flop. The advantage of the D flip flop is that it increases the static power but reduces the dynamic power as well as it will give less energy consumption and less area. This will help us to achieve our goal.

4. CONCLUSIONS AND FUTURE WORK

Most of power is dissipated by links, routers and NI. In all the papers they focused on the power reduction by using encoding technique. The novel encoding technique reduced power 17.34%. the result of novel encoding is compared with BI encoding. The power reduction of novel encoding is better than the BI encoding. SCDBI encoding reduced power 34.67% and area is 8%. But data encoding is more effective as it gives 49% power reduction and also 14% of energy consumption[4]. The praposed shceme gives the advanced architecture and general and transparent with respect to the underlying NoC fabric.experiments carried out on both synthetic and real traffic scenarios show the3 effectiveness of the praposed schemes which allow to save up to more than 51% of the power dissipation and 14% energy consumption without any significant performance degradation and with less than 15% area overhead in the NI.

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